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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,978	07/14/2003	Cha Deok Dong	29936/39473	5905

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EXAMINER	
BERRY, RENEE R	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,978	DONG ET AL.	
	Examiner	Art Unit	
	Renee R Berry	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,465,293 to Park et al. in view of US Patent No. 6,649,965 to Takada et al.

In regards to claim 1, Park teaches a method of manufacturing flash memory device, comprising

the steps of:

(a) sequentially forming a tunnel oxide film, a first polysilicon film and

a hard mask film on a semiconductor substrate;

(b) etching the hard mask film, the

first polysilicon film, the tunnel

through a patterning process to

oxide film and the semiconductor substrate

form a trench within the semiconductor substrate;

(c) depositing an oxide film to bury the trench and then polishing the

oxide film by means of a chemical mechanical polishing process until the hard

mask film is exposed;

(d) removing the hard mask film;

(e) implementing a cleaning process so that a protrusion of the oxide film is recessed to an extent that the sidewall bottom of the first polysilicon film is not exposed;

(f) depositing a second polysilicon film on the results in which the protrusion of the oxide film is recessed and then polishing the second polysilicon film until the protrusion of the oxide film is exposed;

(g) forming a dielectric film on the second polysilicon film; and

(h) forming a control gate on the dielectric film at column 4, lines 2-26

In regards to claim 2, Park teaches the steps of: before the tunnel oxide film is formed on the semiconductor substrate, forming a sacrificial oxide film on the semiconductor substrate; implementing ion implantation for forming wells and ion implantation for controlling the threshold voltage, using the sacrificial oxide film as a buffer layer, and removing the sacrificial oxide film at column 4, lines 27-29.

In regards to claim 3, Park teaches the step of before the step (g) after the step (f), implementing a cleaning process for recessing the oxide film between the second polysilicon films by a given depth in order to increase a contact surface area of the second polysilicon film and the dielectric film at column 4, lines 46-49.

In regards to claim 4, Park teaches the hard mask film is formed using a silicon nitride film having an etch selectivity ratio to the oxide film and is formed in thickness through which the oxide film is protruded sufficiently higher than the surface of the semiconductor substrate at 2, lines 47-52.

In regards to claim 5, Park teaches the oxide film is a HDP oxide film and is deposited in thickness that could be deposited higher than the top surface of the hard mask film while completely burying the trench at column 2, lines 47-51.

In regards to claim 6, Park teaches the cleaning process for recessing the protrusion of the oxide film employs DHF and SC-I solution at column 2, lines 55-61.

In regards to claim 9, Park teaches the control gate is formed to have a dual structure on which a film into which a dopant is doped and a film into which a dopant is not doped are sequentially stacked, in order to prevent diffusion of fluorine (F) that may be substitutionally solidified into a dielectric film to increase the thickness of the oxide film at column 3, lines 19-25.

In regards to claim 11, Park teaches the dielectric film is formed to have a stack structure on which an oxide film, a nitride film and an oxide film are sequentially stacked at column 4, lines 2-25 and column 2, lines 41-65.

However, Park does not teach all the limitations of the claims.

In regards to claims 1 and 7, Takada teaches the first polysilicon film is formed using an amorphous polysilicon film into which a dopant is not doped and wherein the amorphous polysilicon film is formed by means of a 1OW Pressure-chemical vapor deposition (LP-CVD) method using SiH_4 or Si_2H_6 gas at a temperature of 480 - 550 ^{0}C and a low pressure of 0.1 - 3Torr at column 5, lines 1-11.

In regards to claim 8, Takada teaches the second polysilicon film is formed by means of a low pressure-chemical vapor :0 deposition (LP-CVD) method using SiH_4 or

Si_2H_6 gas and PH_3 gas at a temperature of 550 - 620 ^{o}C and a low pressure of 0.1 - 3Torr at column 3, lines 43-44 and column 4, lines 60-67.

In regards to claim 10, Takada teaches the amorphous polysilicon film into which the dopant is doped is formed by a low pressure-chemical vapor deposition (LP-CVD) method using SiH_4 or Si_2H_6 gas and a PH_3 gas at a temperature of 510 - 550 C and a pressure of 0.1 – 3 Torr and the amorphous polysilicon film into which the dopant is not doped by an in-situ process after supply of the PH_3 gas is stopped at column 3, lines 43-44 and column 5, lines 3-15.

In regards to claim 12, Takada teaches the step of before the step (h) after the step (g) implementing a steam anneal process at a temperature of 750 - 800 ^{o}C in order to improve the film quality of the dielectric film and enhance the interface between the stack structure of the oxide film, the nitride film and the oxide film at column 5, lines 46-53.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Park to include the first polysilicon film is formed using an amorphous polysilicon film into which a dopant is not doped and wherein the amorphous polysilicon film is formed by means of a 1OW Pressure-chemical vapor deposition (LP-CVD) method using SiH_4 or Si_2H_6 gas at a temperature of 480 - 550 ^{0}C and a low pressure of 0.1 - 3Torr; the amorphous polysilicon film into which the dopant is doped is formed by a low pressure-chemical vapor deposition (LP-CVD) method using SiH_4 or Si_2H_6 gas and a PH_3 gas at a temperature of 510 - 550 C and a pressure of 0.1 – 3 Torr and the amorphous polysilicon film into which the dopant

is not doped by an in-situ process after supply of the PH_3 gas; and the step of before the step (h) after the step (g) implementing a steam anneal process at a temperature of 750 - 800 ^{o}C in order to improve the film quality of the dielectric film and enhance the interface between the stack structure of the oxide film, the nitride film and the oxide film, since such a modification would result in the miniaturization of the memory cell, as described in column 2, lines 22-25 of Takada et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renee R Berry whose telephone number is (571) 272-1774. The examiner can normally be reached on M-F 9-5:30.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RRB

David Nelms
Supervisory Patent Examiner
Technology Center 2800

June 20, 2004